PATENT ABSTRACTS OF JAPAN

(11)Publication number : **2001-175368**
(43)Date of publication of application : **29.06.2001**

---

(51)Int.CI.

```
G06F  1/32
G06F  1/04
G06F 15/78
```

---

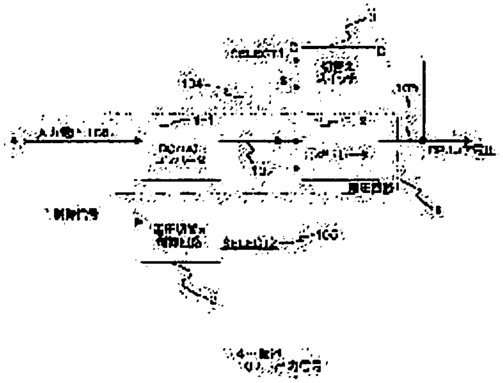
(21)Application number : **11-355264**
(22)Date of filing : **15.12.1999**

(71)Applicant : **NEC SHIZUOKA LTD**
(72)Inventor : **UCHIDA MASANOBU**

---

(54) CPU CORE VOLTAGE SWITCHING CIRCUIT

(57)Abstract:
PROBLEM TO BE SOLVED:To provide a CPU core voltage switching circuit with low power consumption.
SOLUTION:This CPU core voltage switching circuit is provided in a portable information terminal and characterized by setting CPU clock frequency as a half of the one when the portable information terminal is at a state of initial start or an initialized state of memory data when application software is used by the portable information terminal.



LEGAL STATUS

[Date of request for examination]	14.11.2000
[Date of sending the examiner's decision of rejection]	30.04.2002
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	
[Date of registration]	
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

Copyright (C); 1998,2000 Japan Patent Office

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. ******** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention belongs to the core-based-CPU voltage change circuit used for low-power-izing of CPU (arithmetic and program control).

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] Conventionally, especially the core-based-CPU voltage change circuit where this invention is related is used for low-power-izing of CPU. Such a core-based-CPU voltage change circuit is used with a Personal Digital Assistant (PDA) in recent years, and is demanded as low-power-izing as a terminal unit. Conventionally, the core-based-CPU voltage of the circuit of this sort was eternal.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] Conventionally, especially the core-based-CPU voltage change circuit where this invention is related is used for low-power-izing of CPU. Such a core-based-CPU voltage change circuit is used with a Personal Digital Assistant (PDA) in recent years, and is demanded as low-power-izing as a terminal unit. Conventionally, the core-based-CPU voltage of the circuit of this sort was eternal.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] this invention was considered as the composition hung up over below that the above-mentioned technical problem should be solved. The summary of invention according to claim 1 is a core-based-CPU voltage change circuit with which a Personal Digital Assistant is equipped, and when the aforementioned Personal Digital Assistant uses application software, it consists in the core-based-CPU voltage change circuit characterized by making a CPU clock frequency into the frequency of the half when being in an initial starting state and a memory data initialization state. When the aforementioned Personal Digital Assistant uses the aforementioned application software, the summary of invention according to claim 2 By making the aforementioned CPU clock frequency into the frequency of a half in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state Core-based-CPU voltage in case the aforementioned Personal Digital Assistant uses the aforementioned application software It consists in the core-based-CPU voltage change circuit according to claim 1 characterized by controlling to set up so that it may become lower than core-based-CPU voltage in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initialization state. The summary of invention according to claim 3 sets the aforementioned CPU clock frequency to 33MHZ(s), when the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initialization state, and when using the aforementioned application software, it consists in the core-based-CPU voltage change circuit according to claim 1 or 2 characterized by setting the aforementioned CPU clock frequency to 16.5MHZ(s). When the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state, the summary of invention according to claim 4 When core-based-CPU voltage is set as 2.7V and the aforementioned Personal Digital Assistant uses the aforementioned application software by setting the aforementioned CPU clock frequency to 33MHZ(s) It consists in the core-based-CPU voltage change circuit according to claim 1 to 3 characterized by controlling to set core-based-CPU voltage as 2.0V by setting the aforementioned CPU clock frequency to 16.5MHZ(s). A gate means to output input voltage as core-based-CPU voltage according to the arrival of an armature-voltage control signal whose summary of invention according to claim 5 expresses the high voltage, A voltage drop means to reduce input voltage according to the arrival showing a low battery of an armature-voltage control signal, and to output as core-based-CPU voltage, If it is shown according to the control signal inputted into the aforementioned Personal Digital Assistant from the outside that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, the aforementioned CPU clock frequency will be made high. Output the armature-voltage control signal showing the aforementioned high voltage to the aforementioned gate means, and if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software, the aforementioned CPU clock frequency will be made low. It consists in the core-based-CPU voltage change circuit according to claim 1 to 4 characterized by having the voltage change control means which output the armature-voltage control signal showing the aforementioned low battery to the aforementioned voltage drop means. The aforementioned gate means inputs input voltage into a source terminal (S), and the summary of invention according to claim 6 inputs the armature-voltage control signal with which the aforementioned high voltage is expressed to a gate terminal (G), and consists in the core-based-CPU voltage change circuit according to claim 5 characterized by being the field-effect transistor which outputs drain terminal (D) voltage as core-based-CPU voltage. The aforementioned voltage drop means inputs input voltage into an input terminal, and the summary of invention according to claim 7 inputs the armature-voltage control signal which expresses the aforementioned low battery with a control terminal, and consists in the core-based-CPU voltage change circuit according to claim 5 or 6 characterized by being the regulator which outputs output terminal voltage as core-based-CPU voltage. The summary of invention according to claim 8 the aforementioned voltage change control means If it is shown that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, the aforementioned CPU clock frequency will be made high. The hybrid IC which will control the aforementioned CPU clock frequency low if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software, According to the aforementioned CPU clock frequency, if the aforementioned CPU clock frequency is high, the armature-voltage control signal showing the high voltage will be outputted to the aforementioned gate means. If the aforementioned CPU clock frequency is low, it consists in the core-based-CPU voltage change circuit according to claim 5 to 7 characterized by having the RS flip flop and OR circuit which output the armature-voltage control signal showing a low battery to the aforementioned gate means. The summary of invention according to claim 9 consists in the core-based-CPU voltage change circuit according to claim 5 to 8 characterized by equipping the aforementioned hybrid IC with CPU and a system controller. The summary of invention according to claim 10 will set the aforementioned CPU clock frequency to 33MHZ(s), if the aforementioned hybrid IC shows that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, and if the aforementioned control signal shows that it is in the state where the aforementioned application software is used, it consists to the core-based-CPU voltage change circuit according to claim 5 to 9 characterized by controlling the aforementioned CPU clock frequency to 16.5MHZ(s). The summary of invention according to claim 11 consists in the core-based-CPU voltage change circuit according to claim 10 characterized by a gate means outputting input voltage as core-based-CPU voltage of 2.7V according to the arrival showing the high voltage of an armature-voltage control signal. The summary of invention according to claim 12 consists in the core-based-CPU voltage change circuit according to claim 10 or 11 characterized by for a voltage drop means reducing input voltage according to the arrival showing the aforementioned low battery of an armature-voltage control signal, and outputting it as core-based-CPU voltage of 2.0V. The summary of invention according to claim 13 consists in the Personal Digital Assistant equipped with the core-based-CPU voltage change circuit according to claim 1 to 12.

[0005]

[Embodiments of the Invention] this invention circuit drives core-based-CPU voltage for the equipment (for example, Personal Digital Assistant) equipped with this invention circuit by 2.7V at initial during starting and the time of memory data initialization, and drives core-based-CPU voltage by 2.0V at the time of use of application software. When it explains in more detail, for this invention circuit, the equipment equipped with this circuit is CPU at initial during starting and the time of memory data initialization. By setting CLK frequency to f=33MHZ, core-based-CPU voltage is set as 2.7V, and it is CPU at the time of application use. It is the circuit controlled to set core-based-CPU voltage as 2.0V by setting CLK frequency to f/2=16.5MHZ.

[0006] The signal (it becomes the control signal:SUSPEND signal explained later) used as the trigger of a voltage change is controlled by the control signal inputted by the switch of the exterior which is not beforehand illustrated so that it may change, while shifting to an application use screen from initial during starting and the time of memory data initialization by the voltage change control circuit 2 mentioned later. That is, control (key stroke power supply OFF->ON it is the same as that of the mode carried out) turned on after turning off a screen, just before an application screen starts by this switch control was performed, and change control of voltage is mechanically realized depending on this switch control.

[0007] Hereafter, the form of operation of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the form of operation of this invention, and consists of a potential circuit 1, a voltage change control circuit 2, and a changeover switch 3 (it sets in the form of this operation and is an FET:field-effect transistor).

[0008] A potential circuit 1 consists of DC to DC converter 1-1 and a regulator 1-2, as shown in drawing 1 and drawing 2 . Moreover, the voltage change control circuit 2 consists of a hybrid IC 2-1 which consists of CPU 2-101 and a system controller 2-102, and RS flip flop 2-2 and OR circuit 2-3, as shown in drawing 3 .

[0009] Operation of a potential circuit 1 and a changeover switch 3 is explained using drawing 2 and drawing 3 . If input voltage (voltage of a cell 4) is impressed to the input of DC to DC converter (Stepdown) 1-1 (here, referred to as 2.7V) for equipment, an output signal 107 (2.7V) will be outputted to initial during starting (at the time [CLK / CPU / f= 33 MHZ] of a drive). At this time, a regulator 1-2 is an output idle state, and since a changeover switch 3 is in ON state, an output signal 107 is outputted to the core-based-CPU voltage 108 as it is.

[0010] Next, while shifting to an application use screen from initial during starting, the SUSPEND signal (suspension signal) 102 changes and SELECT1 signal 104 and output signal 100 which are an output signal of RS flip flop 2-2 (drawing 3) of the voltage change control circuit 2 change this signal with the control signals from the switch of the exterior which is not illustrated to a trigger. At this time, a changeover switch 3 is in an OFF state, and since a regulator 1-2 is an output state, as for the core-based-CPU voltage 108, the output voltage of a regulator 1-2 is outputted as it is.

[0011] Operation of the voltage change control circuit 2 is explained using drawing 3 . The voltage change control circuit 2 consists of RS flip flops (HC74) 2-2 with the hybrid IC (MCM:Phoenix-HB) 2-1 which consists of CPU 2-101 and a system controller 2-102. The SUSPEND signal 102 and PHNXPWRGD1 signal (reset signal) 103 which are VP3S signal 101 and an output signal of a hybrid IC 2-1 at the input of RS flip flop 2-2 are inputted, respectively.

[0012] RS flip flop 2-2 generates SELECT1 signal 104 and SELECT2 signal 105 which are an output signal of RS flip flop 2-2 in the rising edge of the SUSPEND signal (suspension signal) 102.

[0013] Since the core-based-CPU voltage change circuit concerning the form of operation is constituted like the above, the effect that power consumption can be reduced is done so.

[0014] In addition, in the form of this operation, this invention is not limited to it, but when applying this invention, it is applicable to a suitable form.

[0015] moreover, the above-mentioned composition -- the number of members, a position, a configuration, etc. are not limited to the form of the above-mentioned implementation, but when carrying out this invention, they can be made into a suitable number, a position, a configuration, etc.

[0016] In addition, in each drawing, the same sign is given to the same component.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] Since this invention is constituted as mentioned above, the effect that the core-based-CPU voltage change circuit of a low power can be offered is done so.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention belongs to the core-based-CPU voltage change circuit used for low-power-izing of CPU (arithmetic and program control).
[0002]
[Description of the Prior Art] Conventionally, especially the core-based-CPU voltage change circuit where this invention is related is used for low-power-izing of CPU. Such a core-based-CPU voltage change circuit is used with a Personal Digital Assistant (PDA) in recent years, and is demanded as low-power-izing as a terminal unit. Conventionally, the core-based-CPU voltage of the circuit of this sort was eternal.
[0003]
[Problem(s) to be Solved by the Invention] However, core-based-CPU voltage was eternal, and when the case where CPUCLK (CPU clock) is low-speed-ized as a result, and a load were reduced by the conventional technology, there was a trouble that low-power-ization could not be attained in it. this invention is made in view of this trouble, and the place made into the purpose is in the point of offering the core-based-CPU voltage change circuit of a low power.
[0004]
[Means for Solving the Problem] this invention was considered as the composition hung up over below that the above-mentioned technical problem should be solved. The summary of invention according to claim 1 is a core-based-CPU voltage change circuit with which a Personal Digital Assistant is equipped, and when the aforementioned Personal Digital Assistant uses application software, it consists in the core-based-CPU voltage change circuit characterized by making a CPU clock frequency into the frequency of the half when being in an initial starting state and a memory data initialization state. When the aforementioned Personal Digital Assistant uses the aforementioned application software, the summary of invention according to claim 2 By making the aforementioned CPU clock frequency into the frequency of a half in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state Core-based-CPU voltage in case the aforementioned Personal Digital Assistant uses the aforementioned application software It consists in the core-based-CPU voltage change circuit according to claim 1 characterized by controlling to set up so that it may become lower than core-based-CPU voltage in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initialization state. The summary of invention according to claim 3 sets the aforementioned CPU clock frequency to 33MHZ(s), when the aforementioned Personal Digital Assistant is in an

initial starting state and a memory data initialization state, and when using the aforementioned application software, it consists in the core-based-CPU voltage change circuit according to claim 1 or 2 characterized by setting the aforementioned CPU clock frequency to 16.5MHZ (s). When the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state, the summary of invention according to claim 4 When core-based-CPU voltage is set as 2.7V and the aforementioned Personal Digital Assistant uses the aforementioned application software by setting the aforementioned CPU clock frequency to 33MHZ(s) It consists in the core-based-CPU voltage change circuit according to claim 1 to 3 characterized by controlling to set core-based-CPU voltage as 2.0V by setting the aforementioned CPU clock frequency to 16.5MHZ(s). A gate means to output input voltage as core-based-CPU voltage according to the arrival of an armature-voltage control signal whose summary of invention according to claim 5 expresses the high voltage, A voltage drop means to reduce input voltage according to the arrival showing a low battery of an armature-voltage control signal, and to output as core-based-CPU voltage, If it is shown according to the control signal inputted into the aforementioned Personal Digital Assistant from the outside that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, the aforementioned CPU clock frequency will be made high. Output the armature-voltage control signal showing the aforementioned high voltage to the aforementioned gate means, and if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software, the aforementioned CPU clock frequency will be made low. It consists in the core-based-CPU voltage change circuit according to claim 1 to 4 characterized by having the voltage change control means which output the armature-voltage control signal showing the aforementioned low battery to the aforementioned voltage drop means. The aforementioned gate means inputs input voltage into a source terminal (S), and the summary of invention according to claim 6 inputs the armature-voltage control signal with which the aforementioned high voltage is expressed to a gate terminal (G), and consists in the core-based-CPU voltage change circuit according to claim 5 characterized by being the field-effect transistor which outputs drain terminal (D) voltage as core-based-CPU voltage. The aforementioned voltage drop means inputs input voltage into an input terminal, and the summary of invention according to claim 7 inputs the armature-voltage control signal which expresses the aforementioned low battery with a control terminal, and consists in the core-based-CPU voltage change circuit according to claim 5 or 6 characterized by being the regulator which outputs output terminal voltage as core-based-CPU voltage. The summary of invention according to claim 8 the aforementioned voltage change control means If it is shown that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, the aforementioned CPU clock frequency will be made high. The hybrid IC which will control the aforementioned CPU clock frequency low if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software, According to the aforementioned CPU clock frequency, if the aforementioned CPU clock frequency is high, the armature-voltage control signal showing the high voltage will be outputted to the aforementioned gate means. If the aforementioned CPU clock frequency is low, it consists in the core-based-CPU voltage change circuit according to claim 5 to 7 characterized by having the RS flip flop and OR circuit which output the armature-voltage control signal showing a low battery to the aforementioned gate means. The summary of invention according to claim 9 consists in the core-based-CPU voltage change circuit according to claim 5 to 8 characterized by equipping the aforementioned hybrid IC with CPU and a system controller. The summary of invention according to claim 10 will set the aforementioned CPU clock frequency to 33MHZ(s), if the aforementioned hybrid IC shows that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, and if the aforementioned control signal shows that it is in the state where the aforementioned application software is used, it consists to the core-based-CPU voltage change circuit according to claim 5 to 9 characterized by controlling the aforementioned CPU clock frequency to 16.5MHZ(s). The summary of invention according to claim 11 consists in the core-based-CPU voltage change circuit according to claim 10 characterized by a gate means outputting input voltage as core-based-CPU voltage of 2.7V according to the arrival showing the high voltage of an armature-voltage control signal. The summary of invention according to claim 12 consists in the core-based-CPU voltage change circuit according to claim 10 or 11 characterized by for a voltage drop means reducing input voltage according to the arrival showing the aforementioned low battery of an armature-voltage control signal, and outputting it as core-based-CPU voltage of 2.0V. The summary of invention according to claim 13 consists in the Personal Digital Assistant equipped with the core-based-CPU voltage change circuit according to claim 1 to 12.

[0005]

[Embodiments of the Invention] this invention circuit drives core-based-CPU voltage for the equipment (for example, Personal Digital Assistant) equipped with this invention circuit by 2.7V at initial during starting and the time of memory data initialization, and drives core-based-CPU voltage by 2.0V at the time of use of application software. When it explains in more detail, for this invention circuit, the equipment equipped with this circuit is CPU at initial during starting and the time of memory data initialization. By setting CLK frequency to f=33MHZ, core-based-CPU voltage is set as 2.7V, and it is CPU at the time of application use. It is the circuit controlled to set core-based-CPU voltage as 2.0V by setting CLK frequency to f/2=16.5MHZ.

[0006] The signal (it becomes the control signal:SUSPEND signal explained later) used as the trigger of a voltage change is controlled by the control signal inputted by the switch of the exterior which is not beforehand illustrated so that it may change, while shifting to an application use screen from initial during starting and the time of memory data initialization by the voltage change control circuit 2 mentioned later. That is, control (key stroke power supply OFF->ON it is the same as that of the mode carried out) turned on after turning off a screen, just before an application screen starts by this switch control was performed, and change control of voltage is mechanically realized depending on this switch control.

[0007] Hereafter, the gestalt of operation of this invention is explained with reference to a drawing. Drawing 1 is the block diagram showing the gestalt of operation of this invention, and consists of a potential circuit 1, a voltage change control circuit 2, and a changeover switch 3 (it sets in the gestalt of this operation and is an FET:field-effect transistor).

[0008] A potential circuit 1 consists of DC to DC converter 1-1 and a regulator 1-2, as shown in drawing 1 and drawing 2 . Moreover, the voltage change control circuit 2 consists of a hybrid IC 2-1 which consists of CPU 2-101 and a system controller 2-102, and RS flip flop 2-2 and OR circuit 2-3, as shown in drawing 3 .

[0009] Operation of a potential circuit 1 and a changeover switch 3 is explained using drawing 2 and drawing 3 . If input voltage (voltage of a cell 4) is impressed to the input of DC to DC converter (Stepdown) 1-1 (here, referred to as 2.7V) for equipment, an output signal 107 (2.7V) will be outputted to initial during starting (at the time [CLK / CPU / f= 33 MHZ] of a drive). At this time, a regulator 1-2 is an output idle state, and since a changeover switch 3 is in ON state, an output signal 107 is outputted to the core-based-CPU voltage 108 as it is.

[0010] Next, while shifting to an application use screen from initial during starting, the SUSPEND signal (suspension signal) 102 changes and SELECT1 signal 104 and output signal 100 which are an output signal of RS flip flop 2-2 (drawing 3) of the voltage change control circuit 2 change this signal with the control signals from the switch of the exterior which is not illustrated to a trigger. At this time, a changeover switch 3 is in an OFF state, and since a regulator 1-2 is an output state, as for the core-based-CPU voltage 108, the output voltage of a regulator 1-2 is outputted as it is.

[0011] Operation of the voltage change control circuit 2 is explained using drawing 3 . The voltage change control circuit 2 consists of RS flip flops (HC74) 2-2 with the hybrid IC (MCM:Phoenix-HB) 2-1 which consists of CPU 2-101 and a system controller 2-102. The SUSPEND signal 102 and PHNXPWRGD1 signal (reset signal) 103 which are VP3S signal 101 and an output signal of a hybrid IC 2-1 at the input of RS flip flop 2-2 are inputted, respectively.

[0012] RS flip flop 2-2 generates SELECT1 signal 104 and SELECT2 signal 105 which are an output signal of RS flip flop 2-2 in the rising edge of the SUSPEND signal (suspension signal) 102.

[0013] Since the core-based-CPU voltage change circuit concerning the form of operation is constituted like the above, the effect that power consumption can be reduced is done so.

[0014] In addition, in the form of this operation, this invention is not limited to it, but when applying this invention, it is applicable to a suitable form.

[0015] moreover, the above-mentioned composition -- the number of members, a position, a configuration, etc. are not limited to the form of the above-mentioned implementation, but when carrying out this invention, they can be made into a suitable number, a position, a configuration, etc.

[0016] In addition, in each drawing, the same sign is given to the same component.

[0017]

[Effect of the Invention] Since this invention is constituted as mentioned above, the effect that the core-based-CPU voltage change circuit of a low power can be offered is done so.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1. This document has been translated by computer.So the translation may not reflect the original precisely.
2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The core-based-CPU voltage change circuit which is a core-based-CPU voltage change circuit with which a Personal Digital Assistant is equipped, and is characterized by making a CPU clock frequency into the frequency of the half when being in an initial starting state and a memory data initialization state when the aforementioned Personal Digital Assistant uses application software.
[Claim 2] The core-based-CPU voltage change circuit according to claim 1 characterized by to control to set up so that core-based-CPU voltage in case the aforementioned Personal Digital Assistant uses the aforementioned application software by making the aforementioned CPU clock frequency into the frequency of a half in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state when the aforementioned Personal Digital Assistant uses the aforementioned application software may become low than core-based-CPU voltage in case the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initialization state.
[Claim 3] The core-based-CPU voltage change circuit according to claim 1 or 2 which sets the aforementioned CPU clock frequency to 33MHZ(s) when the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initialization state, and is characterized by setting the aforementioned CPU clock frequency to 16.5MHZ(s) when using the aforementioned application software.
[Claim 4] The core-based-CPU voltage change circuit according to claim 1 to 3 characterized by controlling to set core-based-CPU voltage as 2.0V by setting the aforementioned CPU clock frequency to 16.5MHZ(s) when core-based-CPU voltage is set as 2.7V and the aforementioned Personal Digital Assistant uses the aforementioned application software by setting the aforementioned CPU clock frequency to 33MHZ(s) when the aforementioned Personal Digital Assistant is in an initial starting state and a memory data initial state.
[Claim 5] The core-based-CPU voltage change circuit according to claim 1 to 4 characterized by providing the following. A gate means to output input voltage as core-based-CPU voltage according to the arrival showing the high voltage of an armature-voltage control signal. A voltage drop means to reduce input voltage according to the arrival showing a low battery of an armature-voltage control signal, and to output as core-based-CPU voltage. If it is shown according to the control signal inputted into the aforementioned Personal Digital Assistant from the outside that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, the aforementioned CPU clock frequency will be made high. Output the armature-voltage control signal showing the aforementioned high voltage to the aforementioned gate means, and if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software, the aforementioned CPU clock frequency will be made low. Voltage change control

means which output the armature-voltage control signal showing the aforementioned low battery to the aforementioned voltage drop means.
[Claim 6] The aforementioned gate means is a core-based-CPU voltage change circuit according to claim 5 characterized by being the field-effect transistor which inputs input voltage into a source terminal (S), inputs the armature-voltage control signal with which the aforementioned high voltage is expressed to a gate terminal (G), and outputs drain terminal (D) voltage as core-based-CPU voltage.
[Claim 7] The aforementioned voltage drop means is a core-based-CPU voltage change circuit according to claim 5 or 6 characterized by being the regulator which inputs input voltage into an input terminal, inputs the armature-voltage control signal which expresses the aforementioned low battery with a control terminal, and outputs output terminal voltage as core-based-CPU voltage.
[Claim 8] The core-based-CPU voltage change circuit according to claim 5 to 7 characterized by providing the following. The aforementioned voltage change control means are hybrid ICs which will control the aforementioned CPU clock frequency low if it is shown that it is in the state where will make the aforementioned CPU clock frequency high if it is shown that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, and the aforementioned control signal is using the aforementioned application software. The RS flip flop and OR circuit which will output the armature-voltage control signal showing the high voltage to the aforementioned gate means according to the aforementioned CPU clock frequency if the aforementioned CPU clock frequency is high, and will output the armature-voltage control signal showing a low battery to the aforementioned gate means if the aforementioned CPU clock frequency is low.
[Claim 9] The aforementioned hybrid IC is a core-based-CPU voltage change circuit according to claim 5 to 8 characterized by having CPU and a system controller.
[Claim 10] The aforementioned hybrid IC is a core-based-CPU voltage change circuit according to claim 5 to 9 which will set the aforementioned CPU clock frequency to 33MHZ(s) if it is shown that the aforementioned Personal Digital Assistant has the aforementioned control signal in an initial starting state and a memory data initialization state, and is characterized by controlling the aforementioned CPU clock frequency to 16.5MHZ(s) if it is shown that it is in the state where the aforementioned control signal is using the aforementioned application software.
[Claim 11] A gate means is a core-based-CPU voltage change circuit according to claim 10 characterized by outputting input voltage as core-based-CPU voltage of 2.7V according to the arrival showing the high voltage of an armature-voltage control signal.
[Claim 12] A voltage drop means is a core-based-CPU voltage change circuit according to claim 10 or 11 characterized by reducing input voltage according to the arrival showing the aforementioned low battery of an armature-voltage control signal, and outputting as core-based-CPU voltage of 2.0V.
[Claim 13] The Personal Digital Assistant equipped with the core-based-CPU voltage change circuit according to claim 1 to 12.

[Translation done.]

* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the block diagram of the electrical circuit showing the gestalt of operation of this invention.
[Drawing 2] They are the potential circuit 1 shown in drawing 1 , and an electrical diagram showing a changeover switch 3.
[Drawing 3] It is an electrical diagram showing the internal circuitry of the voltage change control circuit 2 shown in drawing 1 .
[Description of Notations]
1 Potential Circuit
1-1 DC to DC Converter
1-2 Regulator
2 Voltage Change Control Circuit
2-1 Hybrid IC
2-101 CPU
2-102 System controller
2-2 RS Flip Flop
2-3 OR Circuit
3 Changeover Switch
4 Cell
100 Output Signal
101 VP3S Signal
102 SUSPEND Signal
103 PHNXPWRGD1 Signal
104 SELECT1 Signal
105 SELECT2 Signal
106 Input Voltage
107 Output Signal
108 Core-Based-CPU Voltage

[Translation done.]

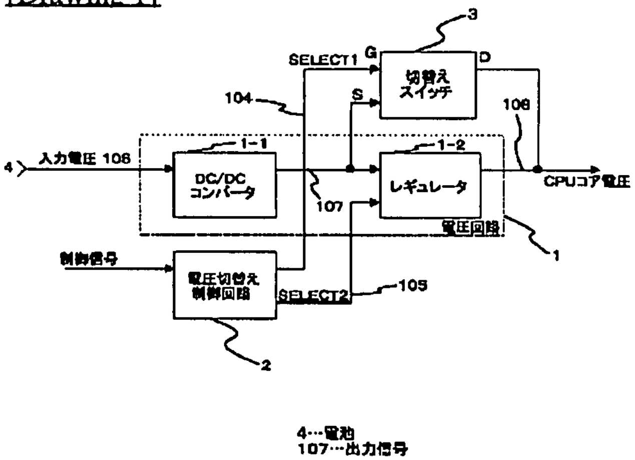
* NOTICES *

Japan Patent Office is not responsible for any
damages caused by the use of this translation.

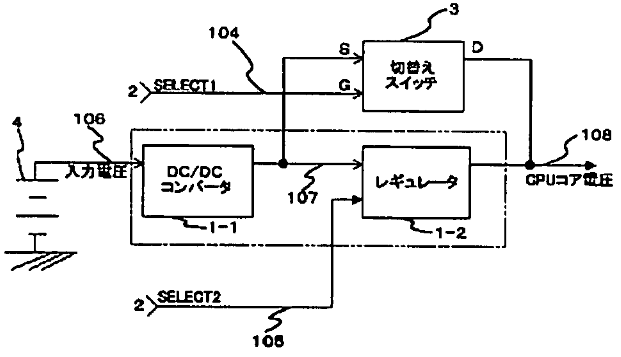
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

[Drawing 1]

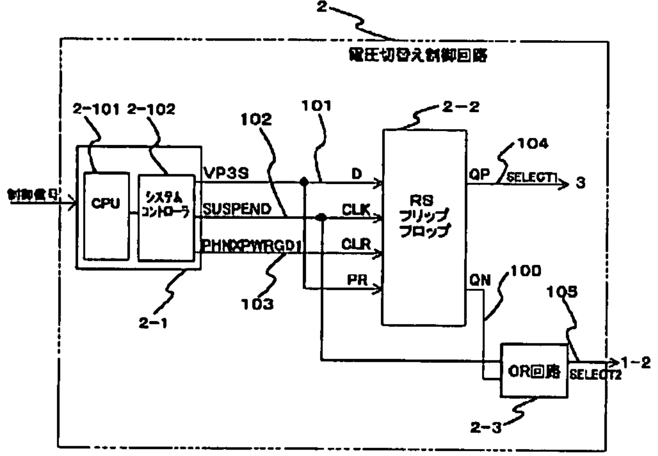

3
SELECT1
G
D
切替え スイッチ
104
S
106
1-1
1-2
4
入力電圧 106
DC/DC コンバータ
レギュレータ
CPUコア電圧
107
電圧回路
1
制御信号
電圧切替え 制御回路
SELECT2
105
2
4…電池
107…出力信号

[Drawing 2]


104
3
S
D
切替え
スイッチ
2
SELECT1
G
4
106
108
入力電圧
DC/DC
コンバータ
107
レギュレータ
CPUコア電圧
1-1
1-2
2
SELECT2
105

1…電圧回路
2…電圧切替え制御回路
4…電池
107…出力信号

[Drawing 3]


2
電圧切替え制御回路
2-101 2-102
102
101
2-2
104
VP3S
D
QP
SELECT1
3
制御信号
CPU
システム
コントローラ
SUSPEND
CLK
RS
フリップ
フロップ
PHNXPWRGD1
CLR
PR
QN
100
105
103
2-1
OR回路
SELECT2
1-2
2-3

1-2…レギュレータ
2-1…混成IC
3…切替えスイッチ
100…出力信号

[Translation done.]